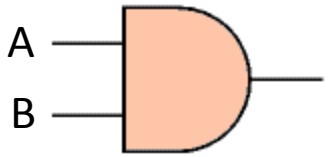
Genetic Logic Circuits

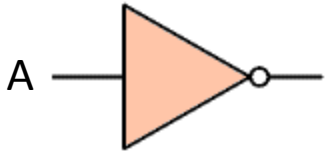
Logic Circuits

AND/NAND



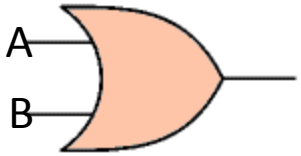
A	B	AND	NAND
1	1	1	0
0	1	0	1
1	0	0	1
0	0	0	1

NOT



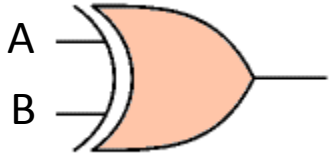
A	B
0	1
1	0

OR/NOR



A	B	OR	NOR
1	1	1	0
0	1	1	0
1	0	1	0
0	0	0	1

XOR/NXOR

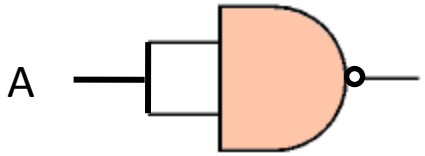


A	B	XOR	NXOR
1	1	0	1
0	1	1	0
1	0	1	0
0	0	0	1

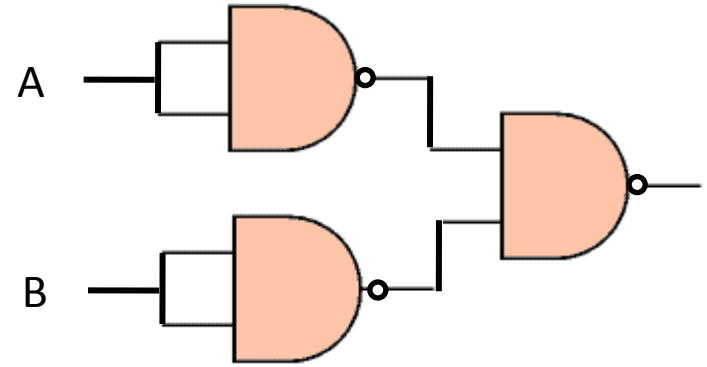
All gates can be derived from the NAND Gate.

OR/NOR/XOR/NXOR/NOT can be Made from Combinations NAND Gates

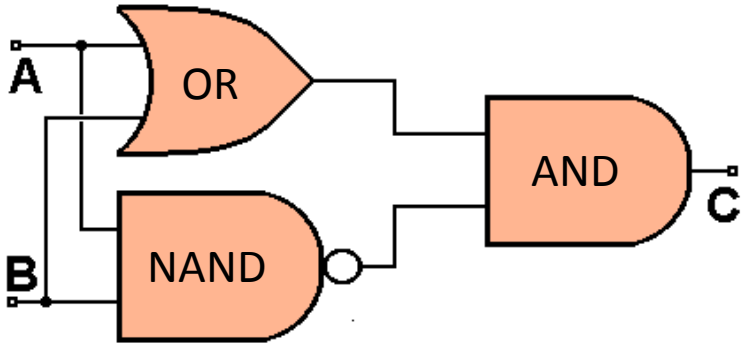
NOT



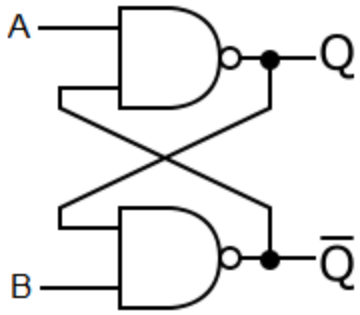
OR

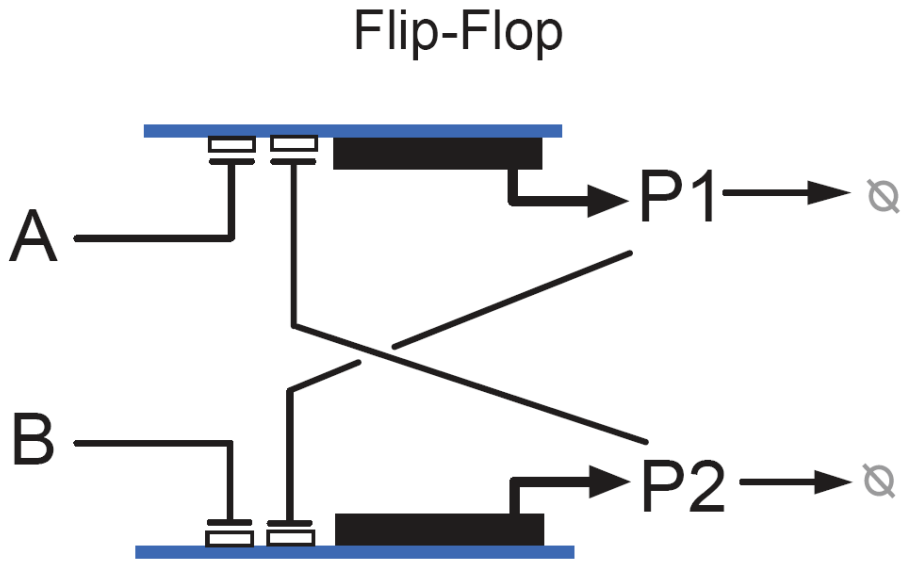


XOR



Flip-Flop (Latch)



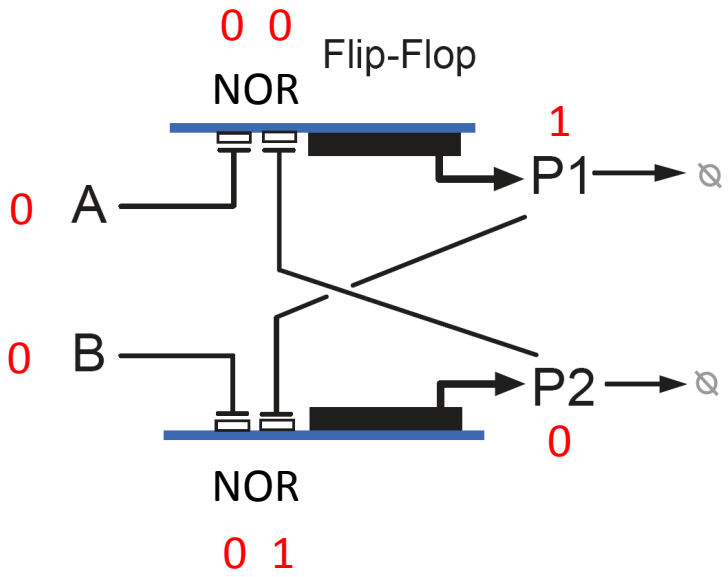


A	B	Q	$\overline{Q}$
1	0	1	0
0	0	1	0
0	1	0	1
0	0	0	1
1	1	0	0

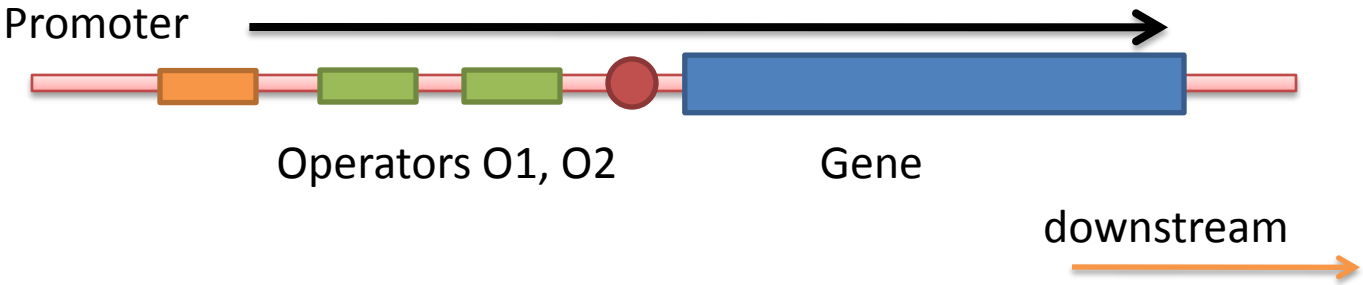
Flip-flops can be made either from NAND or NOR gates. In synthetic biology it is probably easier to construct OR like gates than AND gates.

In addition an OR based flip-flop is quiescent when both inputs are low, meaning low protein levels. Latching occurs when one or other of the inputs is brought to a high state.

Flip-Flop

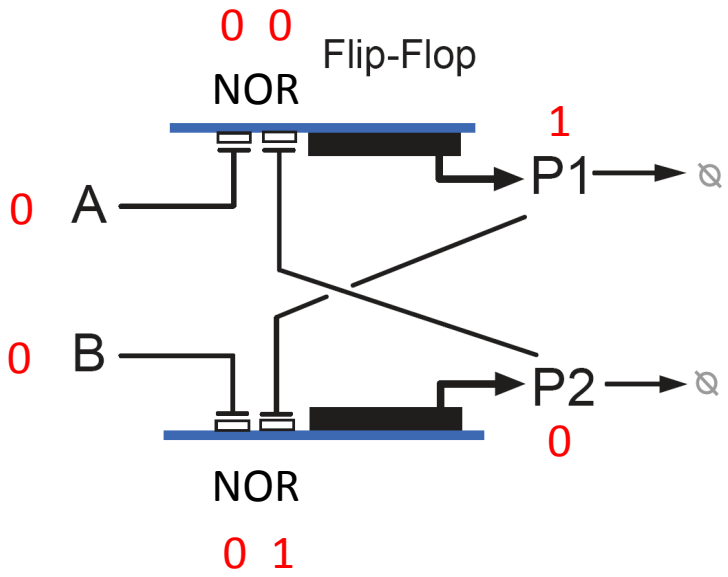


A	B	NOR
1	1	0
0	1	0
1	0	0
0	0	1



Making NOR gates is 'relatively' easy and requires only two operator sites downstream of the RNA polymerase binding site (promoter).

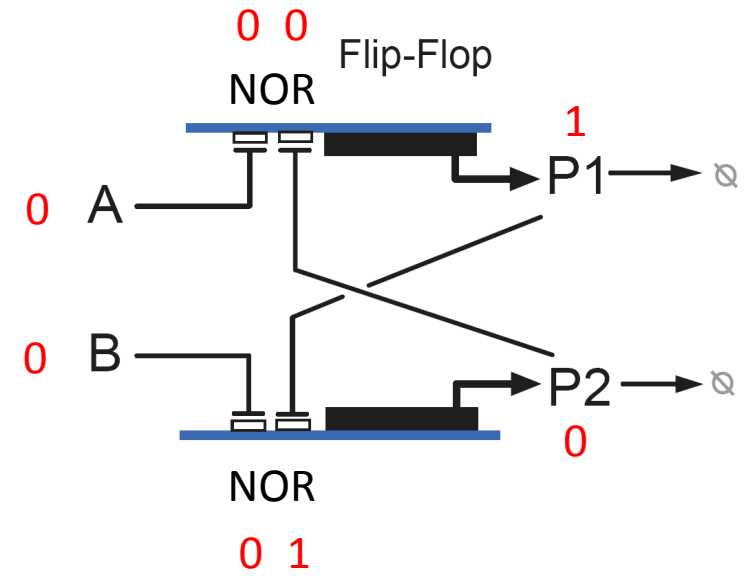
Flip-Flop

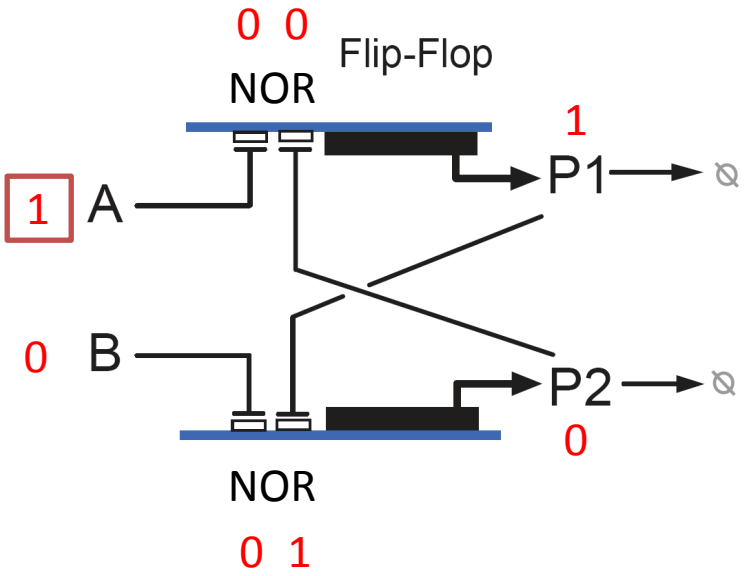


A	B	NOR
1	1	0
0	1	0
1	0	0
0	0	1

Flip-Flop

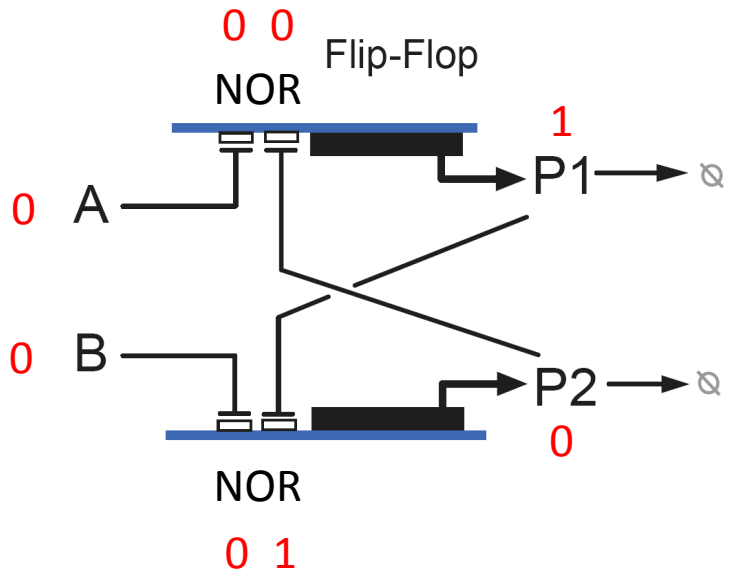
A	B	NOR
1	1	0
0	1	0
1	0	0
0	0	1

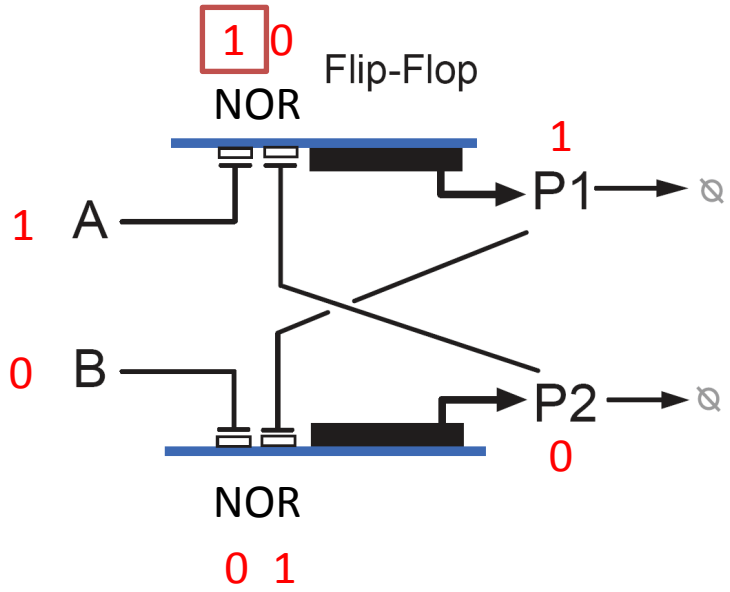




Flip-Flop

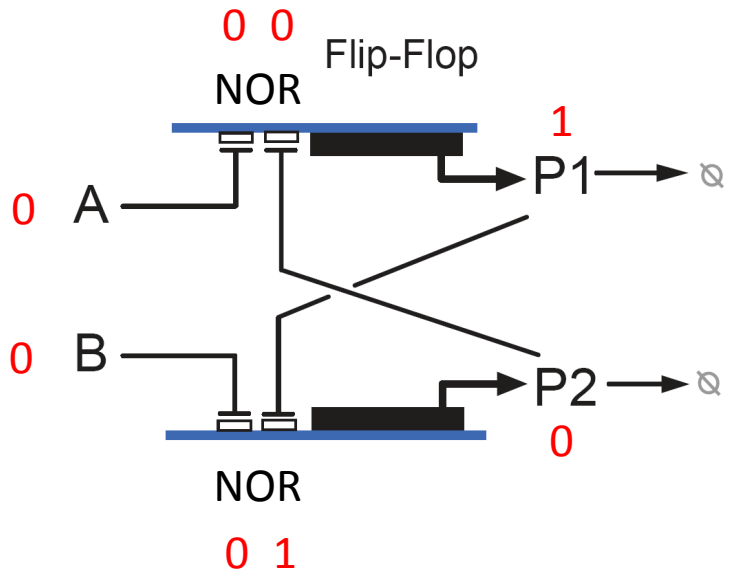
A	B	NOR
1	1	0
0	1	0
1	0	0
0	0	1

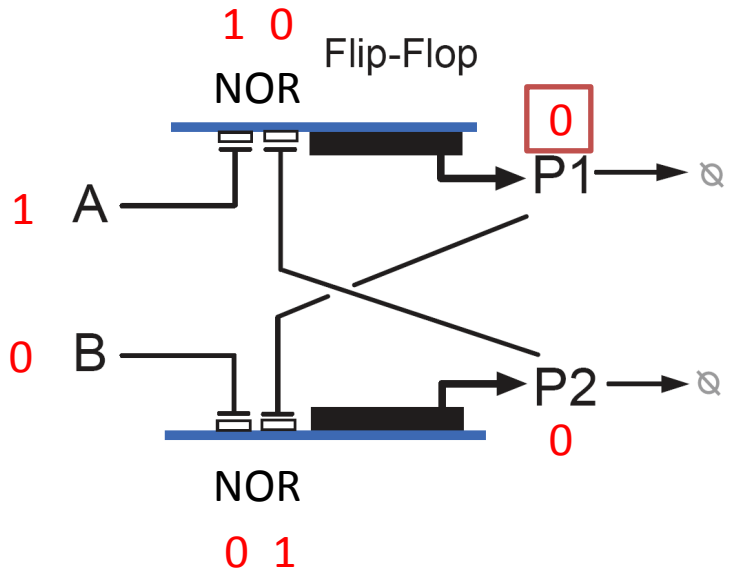




Flip-Flop

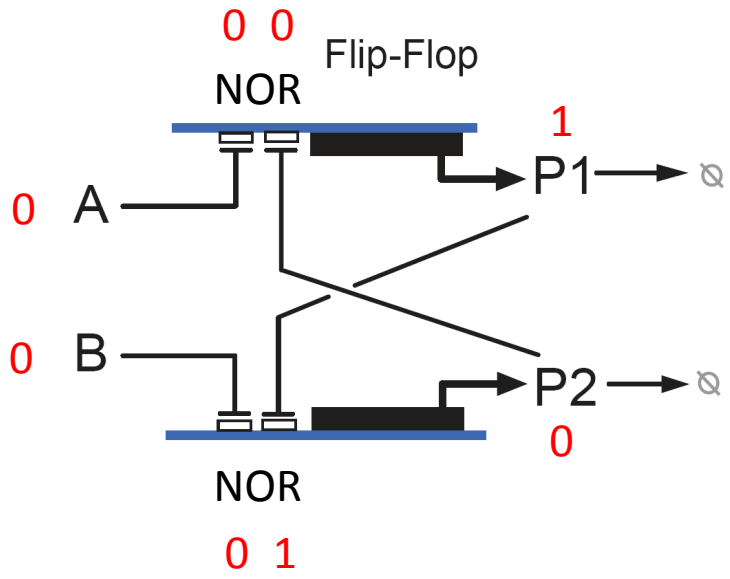
A	B	NOR
1	1	0
0	1	0
1	0	0
0	0	1

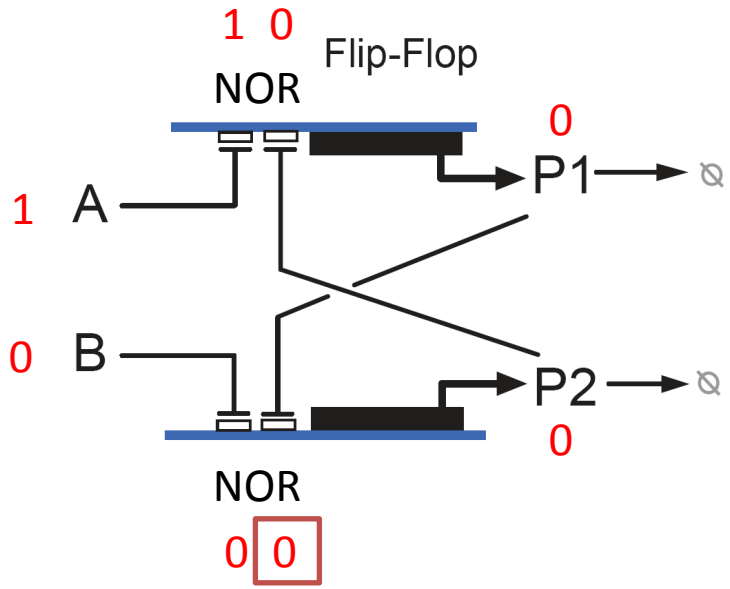




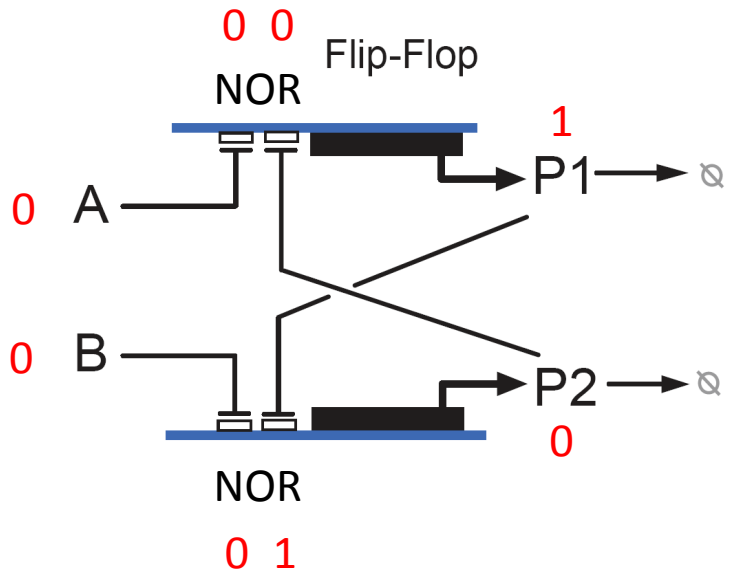
Flip-Flop

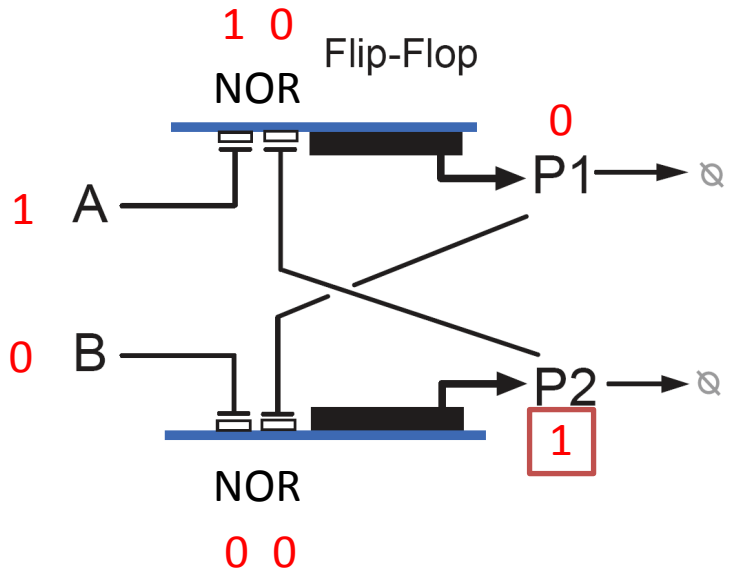
A	B	NOR
1	1	0
0	1	0
1	0	0
0	0	1





Flip-Flop

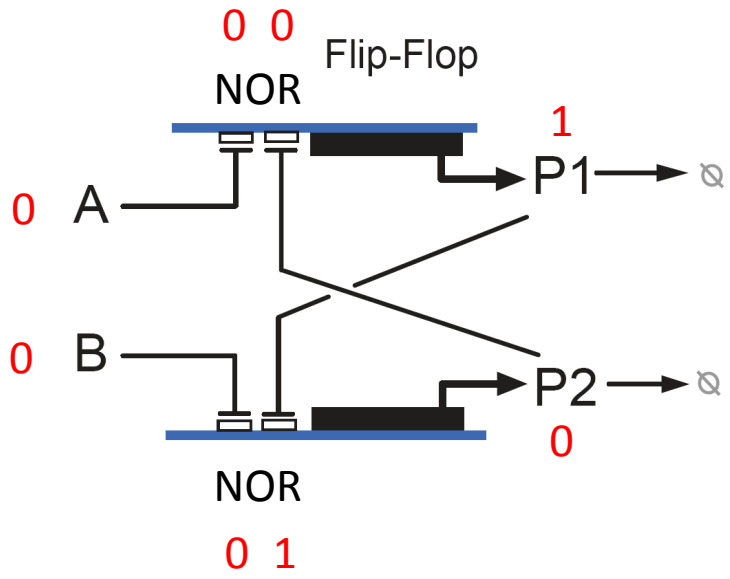


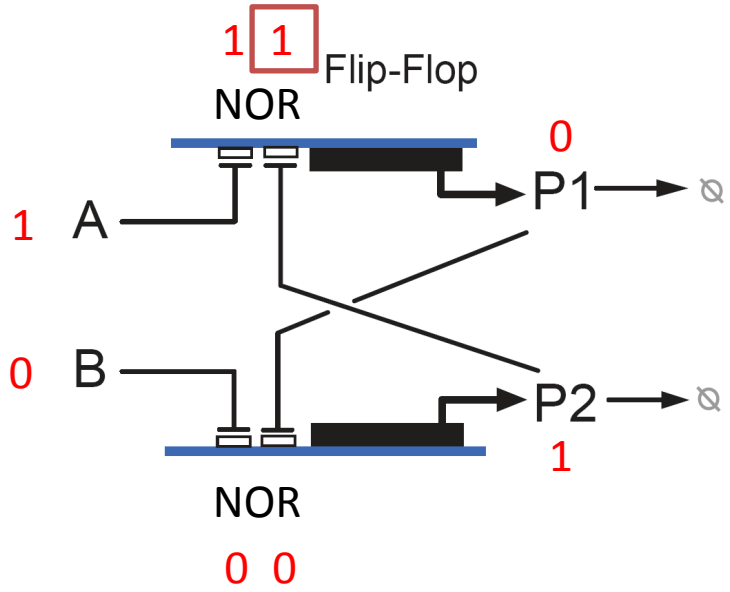


A	B	NOR
1	1	0
0	1	0
1	0	0
0	0	1

Flip-Flop

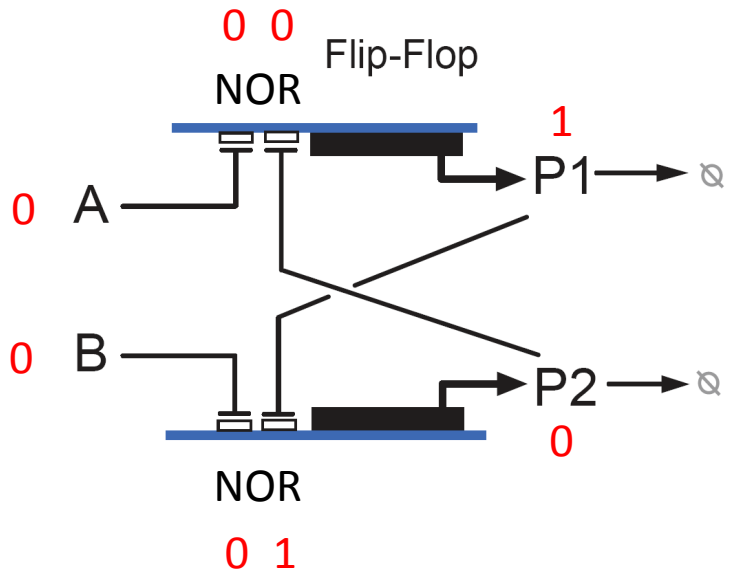
A	B	NOR
1	1	0
0	1	0
1	0	0
0	0	1

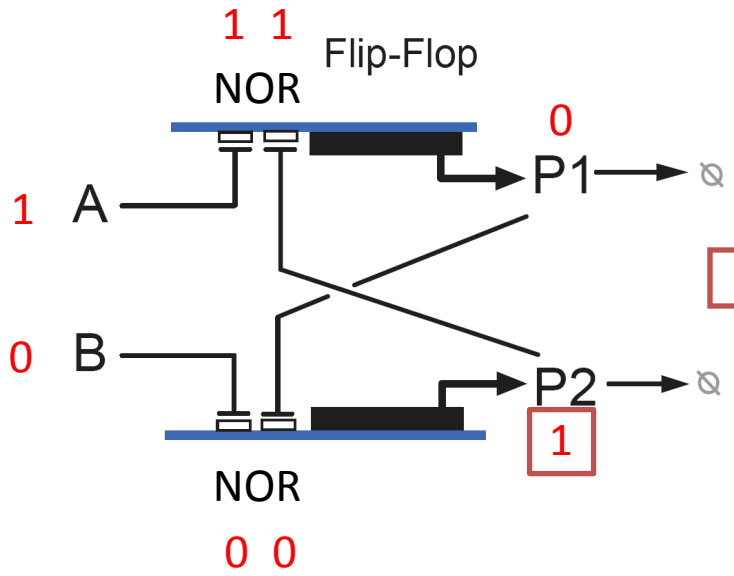


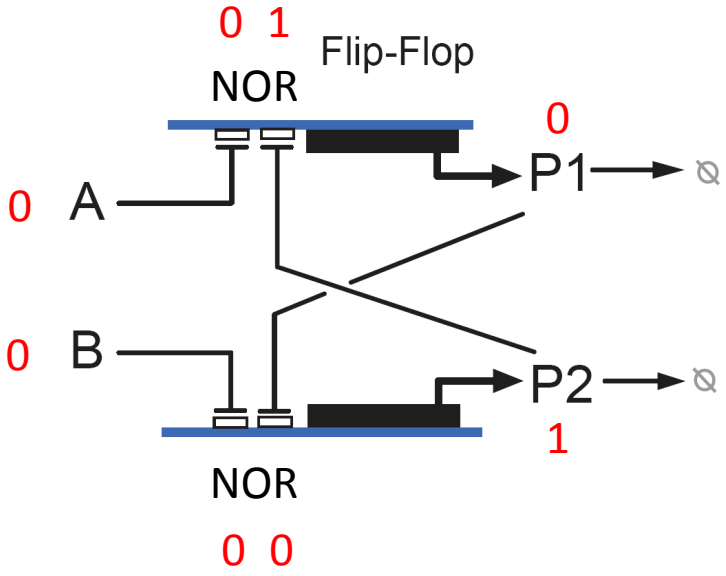


Flip-Flop

A	B	NOR
1	1	0
0	1	0
1	0	0
0	0	1

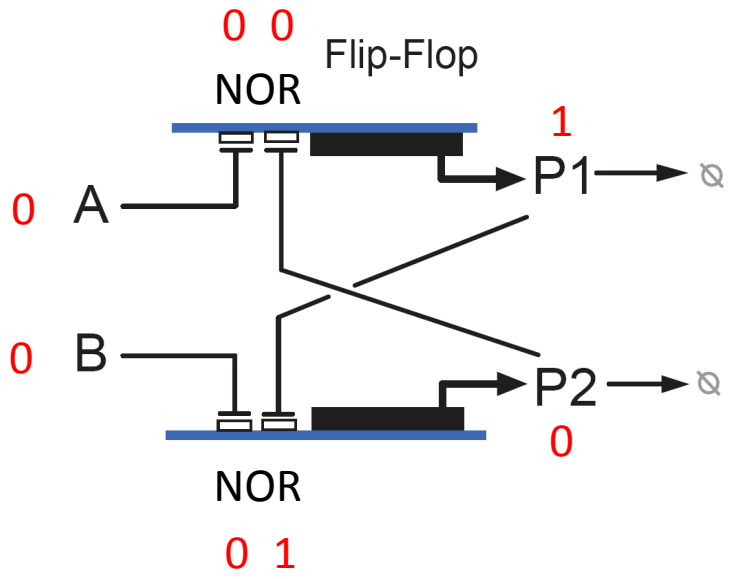




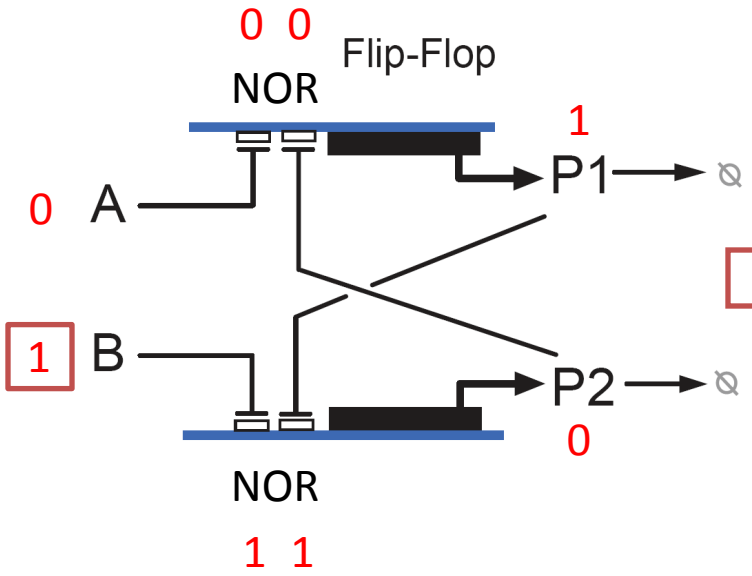


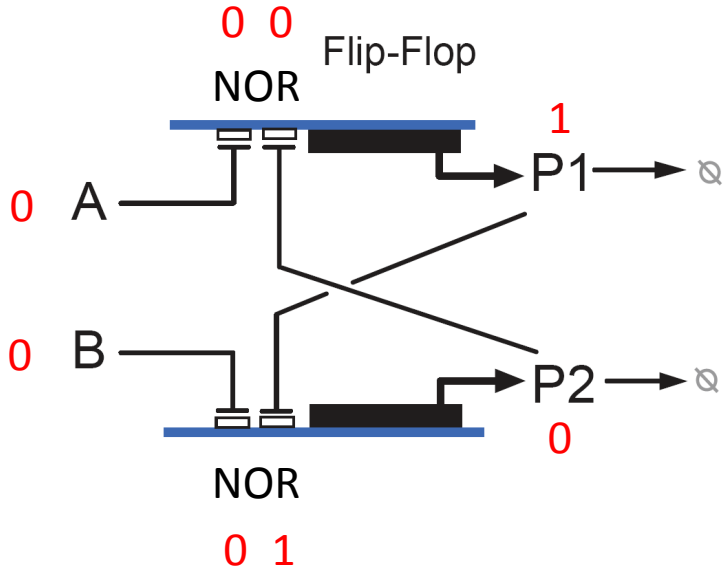
Flip-Flop

A	B	NOR
1	1	0
0	1	0
1	0	0
0	0	1

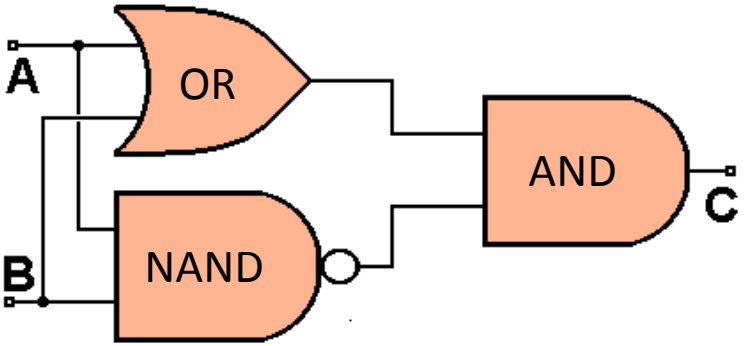


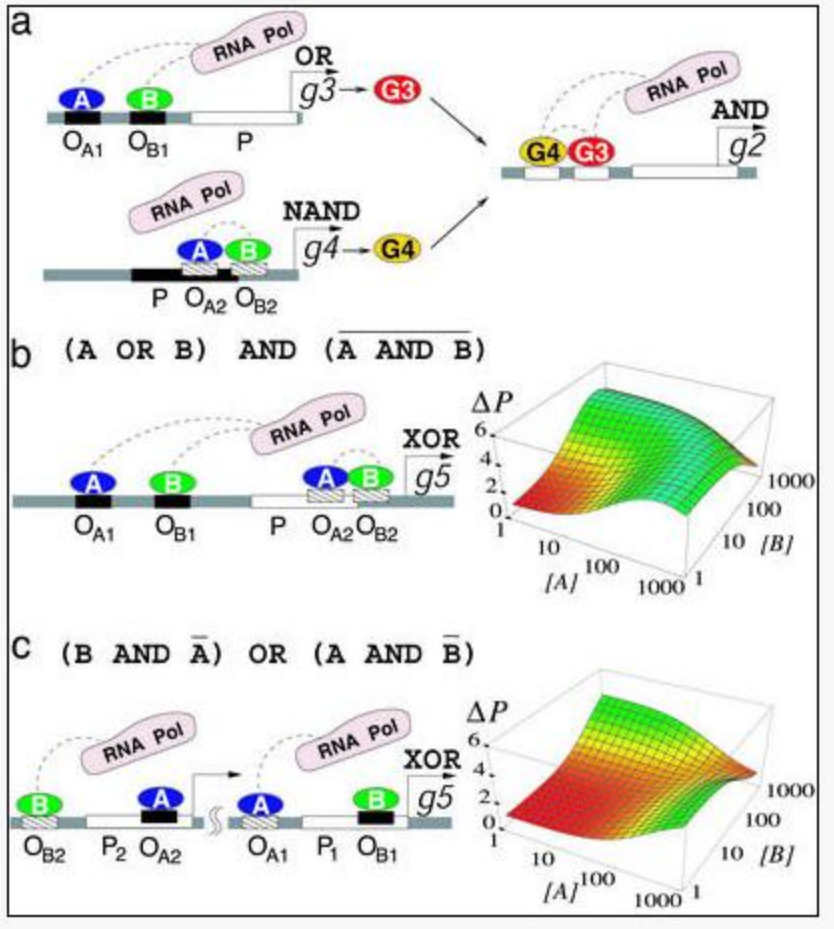
Toggle A to reset P1
Toggle B to set P1





XOR Gate





On schemes of combinatorial transcription logic

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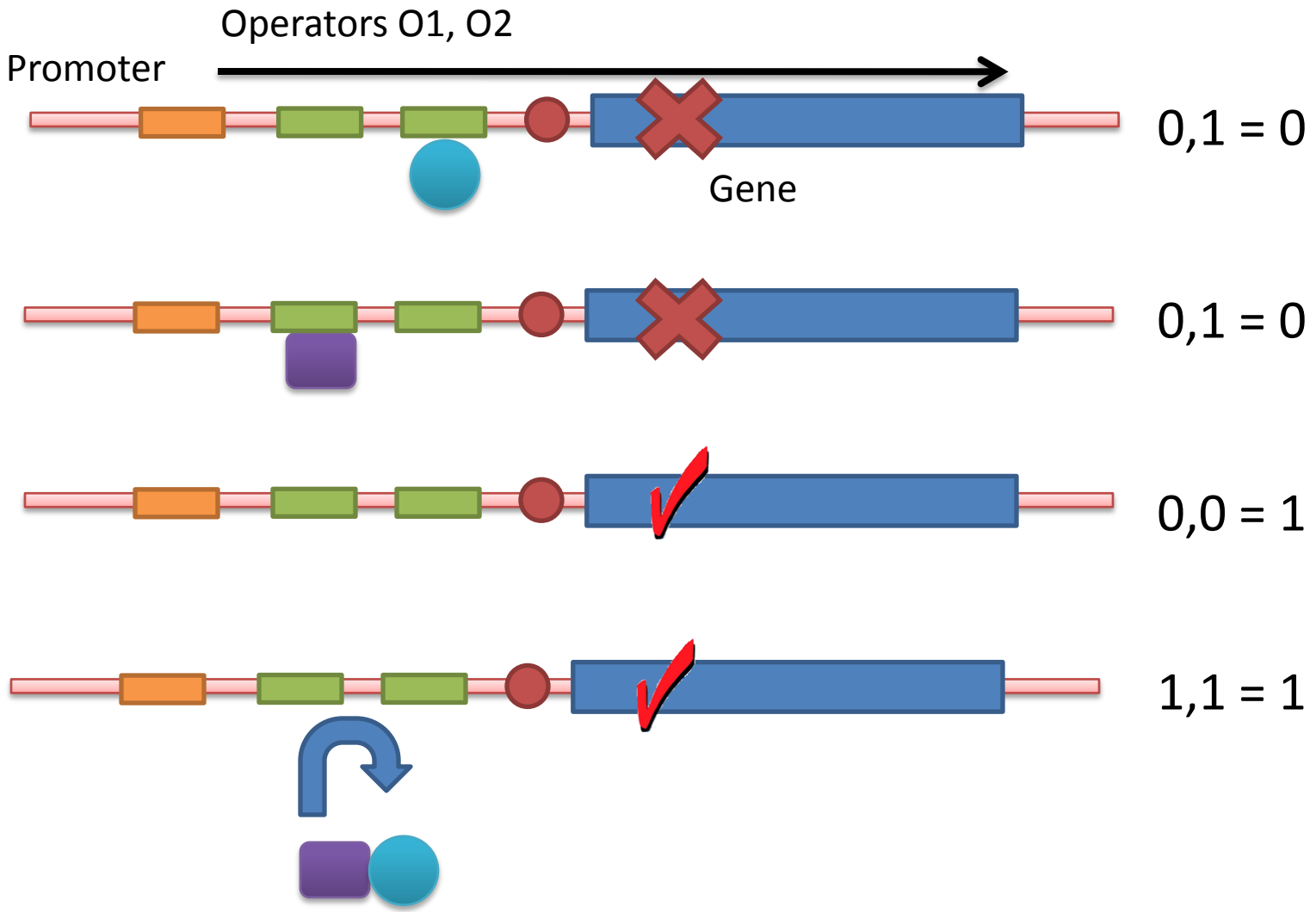
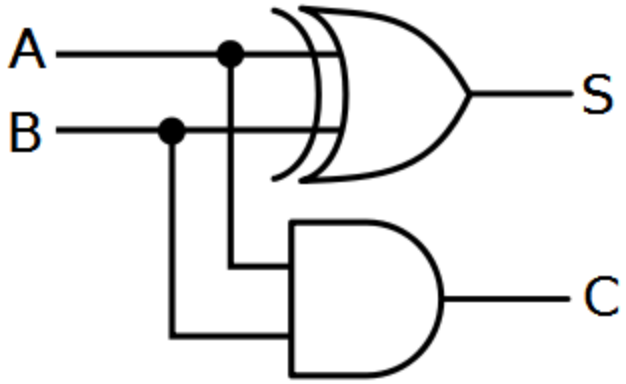
XOR Gate



Half Adder

A	B	S	C
1	1	0	1
0	1	1	0
1	0	1	0
0	0	0	0



0 + 0 = 0

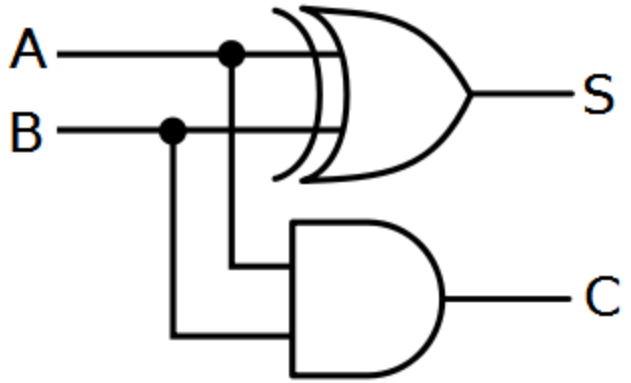
0 + 1 = 1

1 + 0 = 1

1 + 1 = 0 carry 1

Half Adder

A	B	S	C
1	1	0	1
0	1	1	0
1	0	1	0
0	0	0	0



0 + 0 = 0
0 + 1 = 1
1 + 0 = 1
1 + 1 = 0 carry 1

Half-Adder